under ZVS conditions. The power rating of the auxiliary circuit is about one tenth to one fifth that of the main circuit.

![Fig. 3 Operational waveforms of proposed circuit](image)

**Fig. 3** Operational waveforms of proposed circuit

![Fig. 4 Experimental waveforms](image)

**Fig. 4** Experimental waveforms

- (i) load current, 200 A/div
- (ii) primary current, 100 A/div
- (iii) primary voltage of full bridge, 400 V/div
- (iv) terminal voltage of secondary winding of auxiliary transformer: 400 V/div

Timebase: 10 μs/div
- (b) Load current (200 A/div), timebase: 1 s/div
  - (i) short-circuited load
  - (ii) rated load

Proposed circuit: The proposed DC-DC converter is shown in Fig. 1. The left (leading) leg operates under ZCS conditions and the right (lagging) leg operates under ZVS conditions. One cycle operation can be divided into five modes; however, only two modes are shown in Fig. 2. Fig. 3 shows the operation waveforms. The timings of the auxiliary switches ($S_{aux}$, $S_{aux}$) are the same as those of the switches of the lagging leg ($S_1$, $S_2$). During mode 1, switches $S_1$ and $S_2$ are in conduction states and power is transferred through the main transformer and $D_{aux}$ to the load. The secondary terminals of the auxiliary transformer are short-circuited by $D_{aux}$ and $S_{aux}$. Mode 2 is initiated by turning off $S_1$. A resonant circuit is constructed with $C_1$, $C_2$ and $L_1$. The voltage across $S_1$ is increased smoothly to the upper rail voltage, which leads to ZVS turn-off of $S_1$. Similarly switch $S_{aux}$ can be turned off under ZVS conditions. Thereafter mode 3 is initiated. The DC side voltage is reflected to the primary winding of the auxiliary transformer. The reactive energy trapped in the inductor is recovered to the DC side. The primary current decreases to zero, and the load current flows through $D_3$ and $D_4$ evenly. During mode 3, the anti-parallel diode $D_1$ is in conduction, hence $S_1$ can be turned on under ZVS conditions. Similarly, switch $S_{aux}$ can be turned on under ZVS conditions. Thereafter mode 4 is initiated. During this mode the primary current remains zero. Also in this mode the switch $S_1$ is turned off under ZCS conditions and the load current freewheels through the two secondary windings of the transformer. Mode 5 is initiated by turning-on switch $S_2$ under ZCS conditions. The load current flowing through $D_3$ diverts to $D_4$. This mode ends when the current flowing through $D_4$ becomes zero. In this way one switching cycle is completed.

Experimental results: A 10 kW prototype of the proposed circuit has been constructed and tested. The results are shown in Fig. 4. In Fig. 4a, trace (i) is for the load current, trace (ii) is for the primary current of the main transformer, trace (iii) is for the voltage of the full bridge and trace (iv) is for the terminal voltage of the secondary winding of the auxiliary transformer. These waveforms show stable ZVZCS operation. In Fig. 4b, the load current waveform according to the current command is shown. Trace (i) is for a short-circuited load, and trace (ii) is for a rated load. For both load conditions, the desired load currents are obtained.

Conclusion: A new ZVZCS full bridge DC-DC converter suitable for arc welding is proposed. It uses an additional auxiliary transformer to obtain ZCS conditions for the leading leg. The auxiliary circuit including auxiliary transformer is sufficiently small. It operates well over a wide range of the load conditions from no load to short-circuited loads. The operation is verified by experiments. The proposed topology is thought to be suitable for low to high power welding applications due to its simplicity and robustness.

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References


Compensation for nonlinearities in third-generation mobile systems

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A technique for compensating for nonlinear distortion in third-generation (3G) communication systems is presented. In these communication systems, the power-efficient amplification introduces both a widening of the transmitted pulse and nonlinear intersymbol interference. Novel structures are presented which are able to reduce simultaneously both unwanted effects. Examples are presented which show the performance of the compensators in typical digital channels.

Introduction: There is currently a large amount of research effort into finding standards and recommendations which ensure that mobile communications of the future will have access to multi-
media capabilities and service quality similar to that of fixed networks. Recently, different regional standardisation bodies have finalised the specification of the air interface of the universal mobile telecommunications system (UMTS). UMTS terrestrial radio access (UTRA) is based on wideband CDMA (WCDMA) technology [1]. Input bits are spread to the chip rate \( r(1/T_c = 4.096\text{Mchip/s}) \) and subsequently scrambled by a cell-specific scrambling code. QPSK data modulation is used and the pulse shaping filter is a square-root raised cosine (roll-off factor \( \alpha = 0.22 \)). This pulse amplitude modulation (PAM) scheme gives a bandwidth of 5MHz \( (1 + \alpha)T_c = 5\text{MHz} \).

When the transmitter power amplifier is operated in the linear region, the combination of the transmitter and receiver filters produces an ISI-free response. However, under saturation (maximum output power) the amplifier becomes nonlinear and the latter property does not hold. In addition, nonlinear amplification leads to frequency spreading of the transmitted pulse. In practice, this causes severe adjacent channel interference. And, as a result, a degradation in the bit error rate (BER) performance. In short, the channel spacing has to be increased to offset such effects: any spectral efficiency gained by using the (predistorted) PAM scheme may be lost after nonlinear amplification.

**Fractionally-spaced data predistortion:** The conventional symbol-rate data predistorter transforms a finite sequence of \( P \) correlating PAM symbols and produces one predistorted symbol

\[
\begin{align*}
    b[k] &= H(A[k-N_0],...,A[k],...,A[k+M_0]) \\
    &= H(A[k])
\end{align*}
\]

where \( P = N_0 + M_0 + 1 \) is the order of the predistorter. The data predistorter, \( H(\cdot) \), has to be designed in such a way that the correlation of received samples would match (or approximate) the desired PAM signal constellation. The estimation of the received samples is produced by a local receiver placed at the transmitter. It is important to note that predistorters perform better than equalisers (for a given complexity) because the linearisation takes place before the noise is added to the transmitted signal.

Although symbol-rate predistorters are effective at compensating for the warping and clustering effects, they have a limited influence on the transmitted signal spectrum: predistortion every \( T_s \) seconds only allows frequencies below \( 1/T_s \) Hz to be controlled. Our approach is based on predistorting the transmitted symbols so that the received PAM signal approximates the ideal, not only at the maximum eye opening instants, \( sT_e \), but also at the intermediate instants \( kT_e \) where \( k \) is an integer that satisfies \( k \geq 2 \). The suggested system, which provides distortion-free communication at all \( kT_e \) instants, is called a fractionally-spaced data predistorter (FSDP).

Our scheme, depicted in Fig. 1, consists of \( \lambda \) predistorters working in parallel. Each one is trained to approximate the desired sequence at one of the \( \lambda \) intermediate instants. Since all the intermediate values depend on the same sequence of input PAM symbols, the predistorters can be operated at the symbol rate. In this way, the weight addressing/updating algorithms are shared by the \( \lambda \) predistorters, reducing the computational burden of the method.

**GCMAC network:** Predistortion can be interpreted as a function approximation problem. The more accurate the approximation is, the more effective is the compensation for the nonlinear behaviour of the transmission system results. Among the special features of the predistortion function \( H(\cdot) \), we note its multi-dimensional input space (the predistorter must include memory to cope with the nonlinear time dependences), the smoothness (the ideal predistortion functions take similar values at points that are close, in a Euclidean sense, in the input space), and a high dependence on the current transmitted symbol (the contribution of past and future symbols to the predistortion function is considerably smaller).

![Fig. 1 Model of transmission system with data predistortion and pulse shaping](image1)

**Fig. 2 Hardware implementation of GCMAC-based predistorter**

One simple, robust approach is based on the GCMAC network [2]. In the GCMAC algorithm, each input variable (symbol) is quantised into \( L \) discrete values [Note 1]. Each quantised value addresses a fixed memory bank (ROM) that stores pointers to RAM locations (see the block diagram in Fig. 2). Such an indirect addressing scheme satisfies the following rules: the addressed RAM locations must be different for each (quantised) input sample; the number of RAM locations addressed by every input sample must be a constant \( p \) (when \( p = 1 \), the GCMAC becomes an LUT); the group of cells addressed by two consecutive quantised values must only differ in one memory location.

In the update mode, the contents of the addressed memory cells are iteratively improved according to the first-order learning law

\[
\begin{align*}
    w[k+1] &= w[k] + \mu \delta[k] \text{addr}[k]
\end{align*}
\]

where \( \delta[k] \) represents the whole memory bank, \( \text{addr}[k] \) is the error in the approximation and \( \text{addr} \in [0,1]^L \) is the address vector (or association vector) which selects the memory locations to be updated, \( M \) is the size of the RAM bank, and, finally, \( \mu \) is the learning parameter, which takes on a positive value between 0 and 1. In the output-mode, the network produces a linear mixture of all addressed memory cells:

\[
\begin{align*}
    b[k] &= H(w[k],A) = w[k] \text{addr}^T[k]
\end{align*}
\]

The previous addressing algorithm provides the GCMAC network with generalisation capabilities: samples close in Euclidean sense in the input space address similar RAM cells that produce similar output values. In short, the GCMAC network produces smooth output functions that fit the predistortion requirements better than other nonlinear schemes (namely, the Volterra filter and the multilayer perceptron) [3].

**Performance analysis:** The convergence of the GCMAC neural network is achieved only after 2ms (three time slots), for slight nonlinear distortion (OBO = 10dB). This period increases for stronger nonlinearities (six time slots for OBO = 6dB and eight time slots for OBO = 0dB). Also, the mean squared error (MSE) between the original and received samples increases when the amplifier is close to the saturation point, although it remains below the -20dB level.

![Fig. 3a](image2)

**Fig. 3a** illustrates the behaviour of the FSDP in the spectrum domain. Under saturation, the sidelobes of the transmitted power spectrum density (PSD) are 20dB below the main lobe power level. Using an FSDP with an oversampling factor \( \lambda = 16 \) (Fig. 3a), the sidelobes are reduced by 10dB at the adjacent channel.

**Note 1:** The quantisation is not necessary when the input symbols are already discrete in amplitude, as it occurs in predistortion.
frequency (f × T₀ = 1.22). Higher reductions can be achieved by increasing the oversampling factor λ.

Another way to quantify the validity of the proposed predistorters is to compute the equivalent SNR degradation caused by the residual nonlinear distortion at a specified bit error rate (BER).

![Image](image-url)  
**Fig. 3** SNR degradation against output back-off and transmitted power spectrum density

a Total degradation against output back-off for BER = 10⁻⁴  
(i) single channel  
(ii) multichannel (MC)  
(iii) MC, FSDP, λ = 8  
(iv) MC, FSDP, λ = 16  
b Transmitted power spectrum density; λ = 16, OBO = 0dB

Results for BER = 10⁻⁴ are given in Fig. 3b (flat frequency response channel with additive, white, circularly symmetric Gaussian noise is assumed). Using FSDP, the loss in performance with respect to the linear (ideal) system is always less than 1dB (curves (iii), (iv)). The gain, defined as the difference between the minimum values of the SNR degradation, increases when the amplifier operates close to the saturation point. At this point, the gain with respect to the uncompensated transmitter is ~2dB when a single channel configuration is selected, (curve (i)), and above 3dB when two adjacent channels are used (curve (ii)).

**Conclusions:** We have proposed a new structure that predistorts the transmitted signal not only at the symbol instants but also at intermediate instants. By means of λ, GCMAC-based predistorters in parallel, it is possible to obtain a new pulse shape that after the nonlinear processing in the transmission chain produces the desired spectral response. In this way, the proposed data predistorter compensates simultaneously for both the spectral widening and the constellation warping and clustering.

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**References**


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**Experiments on fast cell search algorithm for intercell asynchronous W-CDMA mobile radio**

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Laboratory and field experiment results for a two-step cell search algorithm using scramble code masking for intercell asynchronous W-CDMA mobile radio are presented. The scramble code is masked at different time positions during each scramble period in the forward link common control channel (CCH) for scramble code timing detection at the mobile receiver. 16 scramble codes are used. The cell search time achievable with the authors’ recently proposed three-step cell search algorithm is estimated from the experimental results; cell search can be accomplished within ~960ms at a probability of 93% in the case of 512 scramble codes and 16 scramble code groups.

**Introduction:** Wideband DS-CDMA (W-CDMA) [1] is a promising radio access technique for next generation mobile radio, IMT-2000 [2]. W-CDMA adopts the intercell asynchronous timing concept so that continuous system deployment from outdoors to indoors can be easily realised because no external timing source is required. In intercell asynchronous W-CDMA, all the forward link channels of each cell site are spread by different orthogonal short spreading codes, and then scrambled by a cell-site unique scramble code. A different cell site is assigned a different scramble code. A mobile station must find the best cell site (having the least propagation path loss) and quickly acquire spreading code synchronisation at the beginning of communication. We call this process ‘cell search’. In general, the use of different scramble codes at different cell sites increases the cell search time. To reduce the cell search time, we proposed a novel three-step cell search algorithm in [3], which periodically masks the scramble code in the common control channel (CCH) for scramble code timing detection and parallel-transmits the group identification (GI) code to identify the code group to which the scramble code of the best cell site belongs. For preliminary experiments on the fast cell search algorithm, a two-step cell search algorithm which does not transmit any GI code was implemented. Laboratory and field experiment results on the cell search time are reported in this Letter. Based on the experimental results for the two-step algorithm, the cell search time achievable with a three-step algorithm is estimated.

**Fig. 1 Scramble code masking**

Two-step cell search algorithm and experimental results: The CCH of each cell site is spread by the combination of a cell site-unique scramble code and the common-to-all cell sites short spreading code (CS code), but the scramble code sequence is masked over one data symbol interval at M different time positions during each scramble code period (see Fig. 1) so that the CS code appears M times in each scramble code period. The cell search algorithm is composed of two steps. In the first step, the scramble code masking timing of the best cell site is detected by using a CS code-matched filter. The second step then searches all possible N scramble code candidates.

The above two-step cell search algorithm was implemented in a 4.096Mchip's W-CDMA experiment system. The CCH forward link was quaternary phase shift keying (QPSK) data-modulated, and then QPSK spread. The QPSK data symbol rate in the CCH was 64 ksymbol/s including pilot symbols for coherent detection at the receiver [1]. Orthogonal Gold codes with a repetition period of 64 chips were used to channelise the CCH and traffic channels (TCHs) (the orthogonal Gold code used for the CCH is called a CS code) and a 40900-chip portion of a 2³⁰-chip Gold code was used as the scramble code. The scramble code length was 10ms. A square-root raised cosine Nyquist transmit filter with roll-off